<u>REMARKS</u>

The Office Action dated February 4, 2005, has been received and carefully

noted. The amendments made herein and the following remarks are submitted as a full

and complete response thereto.

Claims 1-14 are pending in the present application and are respectfully submitted

for consideration.

Allowable Subject Matter

As preliminary matter, Applicant appreciates the indication of allowable subject

matter recited in claims 4 and 12, and that they would be allowable if rewritten in

independent form including all of the limitations of the base claim and any intervening

claims.

Claims 1-3, 5-11 and 13-14 Rejected under 35 U.S.C. §103(a)

Claims 1-3, 5-11 and 13-14 were rejected under 35 U.S.C. § 103(a) as being

unpatentable over the Assar et al. (U.S. Patent No. 5,485,595, hereinafter "Assar").

Applicant respectfully traverses the rejection and submits that each of claims 1-3, 5-11

and 13-14 recite subject matter that is neither disclosed nor suggested by the cited prior

art.

Claim 1 recites a nonvolatile semiconductor memory comprising, among other

things, a sub-memory cell array wherein, in case of a rewrite operation rewriting a

portion of data written in the main memory cell array, a modification data is written into

the sub-memory cell array without erasing said main memory cell array, and

correspondent information on a first address of the main memory cell array storing a

2

Application No.: 10/600,767

data to be modified and a second address of the sub-memory cell array storing the

modification data is recorded in the address memory.

Claim 9 recites a nonvolatile semiconductor memory comprising, among other

things, a sub-memory cell array in which, at the time of a rewrite operation modifying a

portion of the first data written in the main memory cell array into a second data, said

modifying second data is written; and an address memory which stores correspondent

information on a first address of the main memory cell array storing a data to be

modified and a second address of the sub-memory cell array storing the second data,

when said second data is written into the sub-memory cell array.

It is respectfully submitted that the prior art fails to disclose or suggest at least

the above-mentioned features of the Applicants' invention.

In making the rejection, the Office Action characterized Assar as allegedly

"showing a non-volatile memory cell array (100) having a plurality of blocks (0-N), and

the use of a separated CAM memory (106) as claimed 'address memory' for holding the

address translation information between a logical address (file 308) and physical

address (408) to be used in accessing the corresponding information inside the memory

array (100)." The Office Action further took the position that "it would have been

obvious to one skilled in this art that, in case of a rewrite operation is needed, a

modification data is written into a new location (983) of the array (100) instead of using

the old location (728)."

Applicant respectfully disagrees with the Office Action's characterization of

Assar.

3

Application No.: 10/600,767

Assar merely discloses a non-volatile content addressable memory (CAM) 106

that is associated with the memory storage 100. The CAM 106 is formed of FLASH

memory or can also be EEPROM. There is one entry in the CAM 106 for every one of

the N blocks in the mass storage 100. Each entry includes a number of fields. The CAM

106 is also formed of a non-volatile memory because loss of its information would make

retrieval of the data files stored in the mass storage 100 impossible.

The logical address 308 portion of the map 108 and the flags 112, 116 and 118

form part of the CAM 106. It is not necessary that the physical address 408 portion of

the map 108 form part of the CAM. Indeed, the physical address 408 portion of the map

108 can be ordinary FLASH memory, EEPROM or even ROM.

Assar further discloses, as an example, that a user is preparing a word

processing document and instructs the computer to save the document. The document

will be stored in the mass storage system as shown in FIG. 1. The computer system will

assign it a logical address 308, for example 526 H. The mass storage system will select

a physical address 408 of an unused block or blocks in the mass storage 100 for storing

the document, e.g. 728 H. That map correlating the logical address 308 to the physical

address 408 is stored in the CAM 106. As the data is programmed, the system of the

previous solution also sets the used/free flag 112 to indicate that this block has been

written without being erased. The used/free flag 112 also forms a portion of the CAM

106. One used/free flag 112 is provided for each entry of the CAM 106.

Further regarding Assar's example, the user retrieves the document, makes a

change and again instructs the computer to store the document. To avoid an erase-

before-write cycle, the system provides means for locating a block having its used/free

4

Application No.: 10/600,767

flag 112 unset (not programmed) which indicates that the associated block is erased.

The system then sets the used/free flag for the new block 114 (FIG. 2) and then stores

the modified document in that new block 114. Next, the system sets the old/new flag

116 of the previous version of the document indicating that this is an old unneeded

version of the document. Lastly, the system updates the correlation between the logical

address 308 and the actual physical address 408. In this way, the system avoids the

overhead of an erase cycle which is required in the erase-before-write of conventional

systems to store a modified version of a previous document.

Applicants submit that Assar fails to disclose or suggest each and every element

recited in claims 1 and 9 of the present application. In particular, it is submitted that

Assar merely discloses a memory storage 100 associated with addressable memory

(CAM) 106, but does not show "a sub-memory cell array" as provided in the present

invention. Furthermore, Assar merely stores the entire modified document in the

memory storage 100 rather than storing only the "modification data" in the sub-memory

cell array in accordance to the present invention. Also, the CAM 106 of Assar stores

the correlating logical address 308 to the physical address 408, but does not store the

correspondence between the first address of the main memory cell array and the

second address of the sub-memory cell array in accordance with the present invention.

Therefore, Applicant submits that Assar fails to disclose each and every element recited

in claims 1 and 9 of the present application.

Moreover, to qualify as prior art under 35 U.S.C. §102, a single prior art

reference must teach, i.e., identically describe, each feature of a rejected claim. As

explained above, Assar fails to disclose or suggest each and every feature of claims 1

5

Application No.: 10/600,767 Attorney Docket No.: 108066-00085

TECH/298610.1

and 9. Accordingly, Applicants respectfully submit that claims 1 and 9 are not

anticipated by Assar. Therefore, Applicant respectfully submits that claims 1 and 9 are

allowable.

As claims 2-3, 5-8, 10-11 and 13-14 are dependent from independent claims 1

and 9, respectively, Applicant submits that each of these claims incorporates the

patentable aspects therein, and are therefore allowable for at least the reasons set forth

above with respect to the independent claims, as well as for the additional subject

matter recited therein.

Accordingly, Applicant respectfully requests withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 1-14

recites subject matter that is neither disclosed nor suggested in the cited prior art.

Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully

request that claims 1-14 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in

condition for allowance, it is respectfully requested that the Examiner contact the

Applicants' undersigned attorney at the indicated telephone number to arrange for an

interview to expedite the disposition of this application.

6

Application No.: 10/600,767

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,

Sam Huang∕

Registration No. 48,430

Customer No. 004372

ARENT FOX KINTNER PLOTKIN & KAHN, PLYC

1050 Connecticut Avenue, N.W.,

Suite 400

Washington, D.C. 20036-5339

Tel: (202) 857-6000 Fax: (202) 638-4810

SH/vdb